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FILE 'USPAT' ENTERED AT 10:37:00 ON 17 DEC 1998

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  *                W E L C O M E   T O   T H E                        *
  *          U. S.   P A T E N T   T E X T   F I L E                  *
  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

=> s stabil? (10a)lead#

        464911 STABIL?
        530346 LEAD#
L1        6625 STABIL? (10A)LEAD#

=> s leadframe# or lead frame#

          1112 LEADFRAME#
        370110 LEAD
        416726 FRAME#
          5652 LEAD FRAME#
                 (LEAD(W)FRAME#)
L2        6317 LEADFRAME# OR LEAD FRAME#

=> s l1 and l2

L3         183 L1 AND L2

=> s (die (3a) pad?) and l3

        111812 DIE
        184932 PAD?
          2694 DIE (3A) PAD?
L4          61 (DIE (3A) PAD?) AND L3

=> s (ceramic# or insulat? or plastic#) and l4

        129079 CERAMIC#
        307921 INSULAT?
        530109 PLASTIC#
L5          56 (CERAMIC# OR INSULAT? OR PLASTIC#) AND L4

=> s (inner or finger#) and l5

        667753 INNER
        155428 FINGER#
L6          47 (INNER OR FINGER#) AND L5

=> s 257/clas

L7       41890 257/CLAS

=> s l6 and l7

L8          32 L6 AND L7

=> d l8 1-32


1.  5,824,950, Oct. 20, 1998, Low profile semiconductor die carrier;
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Joseph M. Mosley, et al., 174/52.4; **257/678** [IMAGE AVAILABLE]

2. 5,821,457, Oct. 13, 1998, Semiconductor die carrier having a dielectric epoxy between adjacent leads; Joseph M. Mosley, et al., 174/52.4; **257/678**; 361/772 [IMAGE AVAILABLE]

3. 5,811,877, Sep. 22, 1998, Semiconductor device structure; Ichiro Miyano, et al., **257/706, 669, 685, 686, 717, 720, 723** [IMAGE AVAILABLE]

4. 5,780,931, Jul. 14, 1998, Surface mounting semiconductor device and semiconductor mounting component; Hiroshi Shimoda, et al., **257/779, 735, 783** [IMAGE AVAILABLE]

5. 5,777,380, Jul. 7, 1998, Resin sealing type semiconductor device having thin portions formed on the leads; Tetsuya Otsuki, et al., **257/675, 674, 706, 707, 796** [IMAGE AVAILABLE]

6. 5,763,952, Jun. 9, 1998, Multi-layer tape having distinct signal, power and ground planes, semiconductor device assembly employing same, apparatus for and method of assembling same; Brian Lynch, et al., **257/735, 666, 668, 692, 696, 713, 758** [IMAGE AVAILABLE]

7. 5,729,049, Mar. 17, 1998, Tape under frame for conventional-type IC package assembly; David J. Corisis, et al., **257/666, 648, 669, 672, 711, 783** [IMAGE AVAILABLE]

8. 5,717,246, Feb. 10, 1998, Hybrid frame with lead-lock tape; Jerry M. Brooks, et al., **257/666, 668, 691** [IMAGE AVAILABLE]

9. 5,708,295, Jan. 13, 1998, **Lead frame** and method of manufacturing the same, and resin sealed semiconductor device and method of manufacturing the same; Akira Oga, et al., **257/676, 666** [IMAGE AVAILABLE]

10. 5,689,135, Nov. 18, 1997, Multi-chip device and method of fabrication employing leads over and under processes; Michael B. Ball, **257/676, 690, 724** [IMAGE AVAILABLE]

11. 5,666,003, Sep. 9, 1997, Packaged semiconductor device incorporating heat sink plate; Kazutaka Shibata, et al., **257/796, 712, 713, 717, 782** [IMAGE AVAILABLE]

12. 5,638,596, Jun. 17, 1997, Method of employing multi-layer tab tape in semiconductor device assembly by selecting, breaking, downwardly bending and bonding tab tape trace free ends to a ground or power plane; John McCormick, 29/827, 835, 844; **257/666** [IMAGE AVAILABLE]

13. 5,633,529, May 27, 1997, Resin sealing type semiconductor device and method of making the same; Tetsuya Otsuki, **257/666, 691, 698, 784** [IMAGE AVAILABLE]

14. 5,619,065, Apr. 8, 1997, Semiconductor package and method for assembling the same; Young S. Kim, **257/673, 674, 692, 696, 790** [IMAGE AVAILABLE]

15. 5,598,034, Jan. 28, 1997, **Plastic** packaging of microelectronic circuit devices; Gene F. Wakefield, **257/706, 707** [IMAGE AVAILABLE]

16. 5,568,363, Oct. 22, 1996, Surface mount components and semifinished products thereof; Akira Kitahara, 361/773; 174/254; **257/676**; 361/776, 803, 813 [IMAGE AVAILABLE]

17. 5,559,369, Sep. 24, 1996, Ground plane for **plastic** encapsulated integrated circuit die packages; Robert A. Newman, **257/668, 676, 747**; 361/765, 771 [IMAGE AVAILABLE]

18. 5,552,631, Sep. 3, 1996, Semiconductor device assembly including power or ground plane which is provided on opposite surface of **insulating** layer from signal traces, and is exposed to central opening in **insulating** layer for interconnection to semiconductor die; John McCormick, **257/666, 668, 692, 696, 713, 734, 735** [IMAGE AVAILABLE]

19. 5,550,406, Aug. 27, 1996, Multi-layer tab tape having distinct signal, power and ground planes and wafer probe card with multi-layer substrate; John McCormick, **257/666, 668, 692, 696, 713, 734, 735** [IMAGE AVAILABLE]

20. 5,455,200, Oct. 3, 1995, Method for making a lead-on-chip semiconductor device having peripheral bond pads; Charles G. Bigler, et al., 29/827; 228/4.5, 180.5, 904; **257/666, 667, 672, 676**; 438/118 [IMAGE AVAILABLE]

21. 5,440,452, Aug. 8, 1995, Surface mount components and semifinished products thereof; Akira Kitahara, 361/773; 174/254, 259; **257/666, 676, 680, 690**; 361/776, 777, 807, 813 [IMAGE AVAILABLE]

22. 5,381,037, Jan. 10, 1995, **Lead frame** with selected **inner** leads coupled to an **inner** frame member for an integrated circuit package assemblies; Jerry Olivarez, **257/666, 676, 678, 691, 778** [IMAGE AVAILABLE]

23. 5,381,036, Jan. 10, 1995, Lead-on chip semiconductor device having peripheral bond pads; Charles G. Bigler, et al., **257/666, 670, 674, 676** [IMAGE AVAILABLE]

24. 5,317,106, May 31, 1994, Coplanar corrector ring; Young I. Kwon, 174/52.4; **257/678**; 361/728, 820 [IMAGE AVAILABLE]

25. 5,289,032, Feb. 22, 1994, Tape automated bonding(tab)semiconductor device and method for making the same; Leo M. Higgins, III, et al., **257/669, 674, 692** [IMAGE AVAILABLE]

26. 5,268,331, Dec. 7, 1993, **Stabilizer**/spacer for semiconductor device **lead frames**; Donald C. Abbott, 427/569; 29/827; **257/671**; 427/576; 438/123 [IMAGE AVAILABLE]

27. 5,250,839, Oct. 5, 1993, Multi-layer **leadframes**, electrically conductive plates used therefor and production of such conductive plates; Kazunori Katoh, et al., **257/666, 669, 674** [IMAGE AVAILABLE]

28. 5,237,205, Aug. 17, 1993, Ground plane for **plastic** encapsulated integrated circuit die packages; Robert A. Newman, **257/783, 668, 676**; 361/765, 771 [IMAGE AVAILABLE]

29. 5,208,188, May 4, 1993, Process for making a multilayer **lead frame** assembly for an integrated circuit structure and multilayer integrated circuit die package formed by such process; Robert A. Newman, 156/310, 273.9; **257/668, 675**; 438/118 [IMAGE AVAILABLE]

30. 5,068,708, Nov. 26, 1991, Ground plane for **plastic** encapsulated integrated circuit die packages; Robert A. Newman, **257/668, 659, 676, 747, 787** [IMAGE AVAILABLE]

31. 4,680,613, Jul. 14, 1987, Low impedance package for integrated circuit die; Wilbert E. Daniels, et al., **257/670, 659, 675, 691, 724** [IMAGE AVAILABLE]

32. 3,767,839, Oct. 23, 1973, **PLASTIC** MICRO-ELECTRONIC PACKAGES; Jack L. Beal, 174/52.3, 16.3, 52.2, 52.4; **257/704**, **730**; 361/291 [IMAGE AVAILABLE]

=> s l6 not l8

L9 15 L6 NOT L8

=> d l9 1-15

1. 5,819,403, Oct. 13, 1998, Method of manufacturing a semiconductor chip carrier; Stanford W. Crane, Jr., et al., 29/841, 842, 845 [IMAGE AVAILABLE]

2. 5,776,802, Jul. 7, 1998, Semiconductor device and manufacturing method of the same; Takao Ochi, et al., 438/123, 106 [IMAGE AVAILABLE]

3. 5,733,800, Mar. 31, 1998, Underfill coating for LOC package; Walter L. Moden, 438/118; 29/827; 264/272.17; 438/123 [IMAGE AVAILABLE]

4. 5,681,777, Oct. 28, 1997, Process for manufacturing a multi-layer tab tape semiconductor device; Brian Lynch, et al., 29/827; 438/122, 123 [IMAGE AVAILABLE]

5. 5,673,845, Oct. 7, 1997, Lead penetrating clamping system; Michael B. Ball, 228/180.5, 44.7, 49.5, 212 [IMAGE AVAILABLE]

6. 5,647,528, Jul. 15, 1997, Bondhead lead clamp apparatus and method; Michael B. Ball, et al., 228/180.5, 49.5, 212 [IMAGE AVAILABLE]

7. 5,639,385, Jun. 17, 1997, Method of fabricating a wafer probe card for testing an integrated circuit die; John McCormick, 216/14; 324/765 [IMAGE AVAILABLE]

8. 5,635,253, Jun. 3, 1997, Method of replenishing electroless gold plating baths; Donald F. Canaperi, et al., 427/437, 443.1 [IMAGE AVAILABLE]

9. 5,362,679, Nov. 8, 1994, **Plastic** package with solder grid array; Gene F. Wakefield, 29/827; 438/122, 123 [IMAGE AVAILABLE]

10. 5,031,821, Jul. 16, 1991, Semiconductor integrated circuit device, method for producing or assembling same, and producing or assembling apparatus for use in the method; Tsuyoshi Kaneda, et al., 228/110.1, 111, 180.5, 219 [IMAGE AVAILABLE]

11. 4,756,080, Jul. 12, 1988, Metal foil semiconductor interconnection method; C. Arthur Thorp, Jr., et al., 29/827; 174/52.4 [IMAGE AVAILABLE]

12. 4,405,242, Sep. 20, 1983, Electronic device and method of fabricating the same; Hideki Kosaka, et al., 368/82, 88; 968/878, DIG.1 [IMAGE AVAILABLE]

13. 4,348,751, Sep. 7, 1982, Electronic device and method of fabricating the same; Hideki Kosaka, et al., 368/82, 87, 88; 968/878, DIG.1 [IMAGE AVAILABLE]

14. 4,010,885, Mar. 8, 1977, Apparatus for accurately bonding leads to a semi-conductor die or the like; Alan S. Keizer, et al., 228/6.2; 226/58; 228/5.5, 105 [IMAGE AVAILABLE]

15. 3,949,925, Apr. 13, 1976, Outer lead bonder; Alan S. Keizer, et al., 228/5.5; 29/827; 228/6.2, 13, 170, 180.21 [IMAGE AVAILABLE]

E003 WORD FREQUENCY SEARCH REPORT

Classification Analysis:

1. 29/827 Total=19 ORs=12 XRs=7
   Class 29 METAL WORKING
   Sub 592 METHOD OF MECHANICAL MANUFACTURE
   Sub 592.1 .Electrical device making
   Sub 825 ..Conductor or circuit manufacturing
   Sub 827 ...Beam lead frame or beam lead device

2. 257/666 Total=16 ORs=6 XRs=10
   Class 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID -STATE DIODES)
   Sub 666 LEAD FRAME

3. 257/676 Total=8 ORs=4 XRs=4
   Class 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID -STATE DIODES)
   Sub 666 LEAD FRAME
   Sub 676 .With structure for mounting semiconductor chip to lead frame (e.g., configuration of die bonding flag, absence of a die bonding flag, recess for LED)

4. 438/123 Total=7 ORs=0 XRs=7
   Class 438 SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS
   Sub 106 PACKAGING (E.G., WITH MOUNTING, ENCAPSULATING, ETC.) OR TREATMENT OF PACKAGED SEMICONDUCTOR
   Sub 121 .Metallic housing or support
   Sub 123 ..Lead frame

5. 257/670 Total=6 ORs=3 XRs=3
   Class 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID -STATE DIODES)
   Sub 666 LEAD FRAME
   Sub 670 .With separate tie bar element or plural tie bars

6. 361/813 Total=6 ORs=3 XRs=3
   Class 361 ELECTRICITY: ELECTRICAL SYSTEMS AND DEVICES
   Sub 600 HOUSING OR MOUNTING ASSEMBLIES WITH DIVERSE ELECTRICAL COMPONENTS
   Sub 679 .For electronic systems and devices
   Sub 813 ..Lead frame

7. 216/14 Total=4 ORs=1 XRs=3
Class 216 ETCHING A SUBSTRATE: PROCESSES
Sub 13 FORMING OR TREATING ELECTRICAL CONDUCTOR ARTICLE (E.G., CIRCUIT, ETC.)
Sub 14 .Forming or treating lead frame or beam lead

8. 257/668 Total=3 ORs=1 XRs=2
Class 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID -STATE DIODES)
Sub 666 LEAD FRAME
Sub 668 .On insulating carrier other than a printed circuit board

9. 257/669 Total=3 ORs=1 XRs=2
Class 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID -STATE DIODES)
Sub 666 LEAD FRAME
Sub 669 .With stress relief

10. 257/672 Total=3 ORs=0 XRs=3
Class 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID -STATE DIODES)
Sub 666 LEAD FRAME
Sub 672 .Small lead frame (e.g., "spider" frame) for connecting a large lead frame to a semiconductor chip

11. 257/677 Total=3 ORs=1 XRs=2
Class 257 ACTIVE SOLID-STATE DEVICES (E.G., TRANSISTORS, SOLID -STATE DIODES)
Sub 666 LEAD FRAME
Sub 677 .Of specified material other than copper (e.g., Kovar (T.M.))

12. 264/272.17 Total=3 ORs=1 XRs=2
Class 264 PLASTIC AND NONMETALLIC ARTICLE SHAPING OR TREATING: PROCESSES
Sub 239 MECHANICAL SHAPING OR MOLDING TO FORM OR REFORM SHAPED ARTICLE
Sub 241 .To produce composite, plural part or multilayered article
Sub 259 ..Shaping material and uniting to a preform
Sub 271.1 ...Preform embedded in or surrounded by shaped material
Sub 272.11 ....Electrical component encapsulating

/964518.sch
Message 3:
From spo_patent@spo.eds.com Fri Jun 5 09:22:45 EDT 1998
Received: from mail1.uspto.gov (mail1.uspto.gov [151.200.97.38]) by shell1.uspto.gov with ESMTP (8.7.1/8.7.1) id JAA09348 for <mayasyst@shell1.uspto.gov>; Fri, 5 Jun 1998 09:22:45 -0400 (EDT)
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Received: from spo.eds.com (www.spo.eds.com [192.238.49.35])
by mail1.uspto.gov (8.8.8/8.8.8) with SMTP id JAA15886
for <mayasyst@shell1.uspto.gov>; Fri, 5 Jun 1998 09:28:53 -0400 (EDT)
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id AA15321; Fri, 5 Jun 1998 08:19:51 CDT
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Status: RO

CUSTOMER REQUEST SUMMARY

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> 1 according 1 added
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> 1 apparent
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> 1 art
> 1 become
> 2 brief
> 1 claims
> 1 conjunction
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> 2 pin
> 3 planarity
> 1 plated
> 6 polyimide

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1 applying
1 background
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Sales Transaction Nbr: 125791
Date Posted: June 5, 1998
Product: E003
Quantity: 50

Sub 272.17 .....Semiconductor or barrier layer device (e.g., integrated circuit, transistor, etc.)

13. 438/118 Total=3 ORs=0 XRs=3
Class 438 SEMICONDUCTOR DEVICE MANUFACTURING: PROCESS
Sub 106 PACKAGING (E.G., WITH MOUNTING, ENCAPSULATING, ETC.) OR TREATMENT OF PACKAGED SEMICONDUCTOR
Sub 118 .Including adhesive bonding step

Patent Report:

Ref	Patent Id	Issue/File	US Class (OR)	Title
1	05352633	Oct 4 1994 Jun 2 1992	156/233	Semiconductor lead frame lead stabilization

Inventor: Abbott; Donald C.
Assignee: Texas Instruments Incorporated
Abstract:
The invention is to an apparatus and method for applying a plastic material to a lead frame for stabilizing the leads and retaining them in a common plane.

Ref	Patent Id	Issue/File	US Class (OR)	Title
2	05496435	Mar 5 1996 Jul 13 1994	156/556	Semiconductor lead frame lead stabilization

Inventor: Abbott; Donald C.
Assignee: Texas Instruments Incorporated
Abstract:
The invention is to an apparatus and method for applying a plastic material to a lead frame for stabilizing the leads and retaining them in a common plane.

Ref	Patent Id	Issue/File	US Class (OR)	Title
3	05268331	Dec 7 1993 Jan 7 1992	427/569	Stabilizer/spacer for semiconductor device lead frames

Inventor: Abbott; Donald C.
Assignee: Texas Instruments Incorporated
Abstract:
The invention is to a method for plasma spraying a ceramic or plastic material on selected areas of leads to form stabilizer/spacers for the leads.

Ref	Patent Id	Issue/File	US Class (OR)	Title
4	05561320	Oct 1 1996 Oct 25 1994	257/677	Silver spot/palladium plate lead frame finish

Inventor: Abbott; Donald C. et al.
Assignee: Texas Instruments Incorporated

Abstract:

A lead frame is plated with palladium and then selected portions of the lead frame leads are spot plated with silver to improve solderability.

5 04868635 Sep 19 1989 257/667 Lead frame for integrated circuit
Jan 13 1988

Inventor: Frechette; Raymond A. et al.

Assignee: Texas Instruments Incorporated

Abstract:

An integrated circuit lead frame is configured so that it may be die stamped to cut lead frame leads to customize it for a particular semiconductor device bar size. Lead frame leads are cut at a specified distance from the lead frame bar pad so that a semiconductor device bar which is larger than the bar pad may be mounted on the bar pad and cut segments of lead frame leads that are attached to the bar pad.

6 05384155 Jan 24 1995 427/125 Silver spot/palladium plate lead
Jun 4 1992 frame finish

Inventor: Abbott; Donald C. et al.

Assignee: Texas Instruments Incorporated

Abstract:

The invention is to a method of spot plating parts of a plated semiconductor lead frame. The entire lead frame is first plated. Then parts of the lead frame, internal to the subsequent encapsulating package, are spot plated prior to encapsulating the semiconductor device. A spot of silver is plated in the mount and/or bond area of the lead frame.

7 04279682 Jul 21 1981 156/367 Apparatus for securing tape to
Nov 2 1979 leads of semiconductor lead frame

Inventor: Hamagami; Teruaki et al.

Assignee: Sumitomo Metal Mining Company Limited

Abstract:

An apparatus for securing a tape to leads of a semiconductor lead frame, includes, a tape feeder, a punch for punching the tape and for pressing the punched tape against the lead frame, a mechanism for horizontally moving the lead frame and setting it in the punch and the press, and a mechanism for adjusting the timing of the feeder, the punch, the press and the moving mechanism. The punch and the press include a fixed upper die on which the lead frame rests and in which the tape is supported, the punch being movable against the tape for punching out a portion of the tape and for pressing it against the lead frame.

8 05308797 May 3 1994 438/127 Leads for semiconductor chip
Nov 24 1992 assembly and method

Inventor: Kee; David R.

Assignee: Texas Instruments Incorporated
Abstract:
A semiconductor device is formed without using a leadframe. A semiconductor device is formed in one area of a semiconductor chip and a second area includes conductors to which lead wires are bonded. The lead wires are used for mounting the semiconductor device.

9 05594234 Jan 14 1997 257/676 Downset exposed die mount pad leadframe and package
Nov 14 1994
Inventor: Carter, Jr.; Buford H. et al.
Assignee: Texas Instruments Incorporated
Abstract:
The invention is a single piece deep downset exposed lead frame (10) that can be used in current production processes. A single lead frame (10) has a die mount pad (12) that is formed with a downset or cavity into which the semiconductor die (20) is mounted. Wings (14, 15, 17, 18) lock the die pad in the device package (21) and increase the length of potential moisture paths (34a). The downset die pad (12) provides direct thermal contact of the die mount pad (12) to an external heat sink, eliminating the need for a heat slug internal to the package. The exposed die pad (12) can also be used as an RF ground connection to an RF circuit ground plane.

10 05480519 Jan 2 1996 205/661 Electrochemical etch system and method
Feb 6 1995
Inventor: Abbott; Donald C. et al.
Assignee: Texas Instruments Incorporated
Abstract:
A method and apparatus for forming lead frames and eliminating irregularities in the edge (22) of openings etched in the sheet metal from which the lead frame is formed. In a first process, a photo resist coated metal sheet (36) is first etched by a photo chemical process to define the lead frame, and then the lead frame metal sheet (36) is etched in an electrochemical process to remove edge irregularities. In a second process, the entire lead frame is formed in an electrochemical process.

11 05558267 Sep 24 1996 228/4.5 Moat for die pad cavity in bond station heater block
Mar 31 1995
Inventor: Humphrey; Henry L. et al.
Assignee: Texas Instruments Incorporated
Abstract:
A wire bond station has a platform (32) in cavity (31) of the work station heater block (30) on which a lead frame die mount pad (33) is placed during wire bonding to semiconductor chip mounted on the die mount pad. The platform (32) is of a dimension such that the edges of the die

mount pad (33) extend out from the platform (32) so that irregularities (34) on the edges of the die mount pad (33) do not support the die mount pad (33) above the platform (32).

12 05610437 Mar 11 1997 257/670 Lead frame for integrated circuits
May 25 1994
Inventor: Frechette; Raymond A.
Assignee: Texas Instruments Incorporated
Abstract:
This invention relates to lead frames upon which chips are mounted prior to encapsulation. A lead frame structure (6) for manufacturing an IC device comprises a lead frame base (1) including a plurality of leads (10) and four first tie bar portions (16) extending toward a die pad aperture (17). A die pad (2) forms a mounting surface (20) for receiving a chip (30) and includes four second tie bar portions (21) extending from the mounting surface (20) and corresponding to the four first tie bar portions (16). The die pad (2) is affixed to the lead frame base (1) and positioned in the aperture (17) by affixing each of the second tie bar portions (21) to a corresponding one of the first tie bar portions (16).

13 05097406 Mar 17 1992 364/167.01 Lead frame lead located for wire
Oct 3 1989 bonder
Inventor: Narasimhan; Mandayam A. et al.
Assignee: Texas Instruments Incorporated
Abstract:
A lead frame locater is used to locate actual positions of lead frame leads in respect to the semiconductor chip to provide accurate wire bonding of the semiconductor chip to the lead frame leads.

14 05343615 Sep 6 1994 29/827 Semiconductor device and a process
Mar 19 1992 for making same having improved
leads
Status: certificate of correction has been issued
Inventor: Sono; Michio et al.
Assignee: Fujitsu Limited
Abstract:
A process for producing a semiconductor device having a package with a semiconductor element molded therein, and a plurality of leads, each constituted by an inner lead located inside the package and an outer lead located outside the package, the leads being arranged in a line at a predetermined pitch, and the semiconductor element being electrically connected to the inner lead of each of the leads, wherein each side edge of each of the outer leads is flat.

15 05452511 Sep 26 1995 29/827 Composite lead frame manufacturing

Nov 4 1993 method

Inventor: Chang; Alexander H. C.

Abstract:

A method for constructing a composite lead frame (10) wherein a plurality of lead segments (14) are separately constructed and then attached to a frame member (12). A plurality of the frame members (12) may optionally be produced as a lead frame strip (16). Each of the frame members (12) has an opposed pair of side rails (18) and a pair of cross members (20) for enclosing a lead area (22) wherein the lead segments (14) are affixed to the side rails (18) and the cross members (20) by a plurality of assembly tabs (40).

16 05633206 May 27 1997 29/827 Process for manufacturing lead
Nov 14 1995 frame for semiconductor package

Inventor: Kim; Sang H. et al.

Assignee: Samsung Electronics Co., Ltd.

Abstract:

A process for manufacturing a lead frame having a pad, inner leads, outer leads and dambars, the lead frame being coated with a film on the back surface of the pad, which includes the steps of preparing a lead frame having a pad, inner leads and outer leads; placing a polyamic acid film on the back surface of the pad without using adhesive; and thermally compressing the polyamic acid film by using a heat; generator, to form polyimide film and simultaneously adhere that to the polyimide film the back surface of the pad.

17 05471369 Nov 28 1995 361/813 Semiconductor device having a
Mar 17 1994 plurality of semiconductor chips

Status: certificate of correction has been issued

Inventor: Honda; Tosiyuki et al.

Assignee: Fujitsu Limited et al.

Abstract:

A chip-on chip type semiconductor device is provided in which semiconductor chips provided in a package cannot be displaced during a transfer molding process so as to eliminate a short circuit. At least two lead frames are provided in and extend from the package so that the first semiconductor chip and the second semiconductor chip can be electrically connected to external devices. A die stage is provided between the first semiconductor chip and the second semiconductor chip. A bonding wire is provided for wiring between the first semiconductor chip and the lead frames, and TAB leads connect the second semiconductor chip to the lead frames. The lead frames may extend between the first and second semiconductor devices instead of the die stage. The lead frames may include one having a portion extending in a direction perpendicular to the longitudinal direction of the lead frames between the first and second

semiconductor chips.

18 05579208 Nov 26 1996 361/813 Semiconductor device having a
Jun 2 1995 plurality of semiconductor chips
Status: certificate of correction has been issued
Inventor: Honda; Tosiyuki et al.
Assignee: Fujitsu Limited et al.
Abstract:

A chip-on chip type semiconductor device is provided in which semiconductor chips provided in a package cannot be displaced during a transfer molding process so as to eliminate a short circuit. At least two lead frames are provided in and extend from the package so that the first semiconductor chip and the second semiconductor chip can be electrically connected to external devices. A die stage is provided between the first semiconductor chip and the second semiconductor chip. A bonding wire is provided for wiring between the first semiconductor chip and the lead frames, and TAB leads connect the second semiconductor chip to the lead frames. The lead frames may extend between the first and second semiconductor devices instead of the die stage. The lead frames may include one having a portion extending in a direction perpendicular to the longitudinal direction of the lead frames between the first and second semiconductor chips.

19 05724233 Mar 3 1998 361/813 Semiconductor device having first
May 15 1996 and second semiconductor chips
with a gap therebetween, a die
stage in the gap and associated
lead frames disposed in a package,
the lead frames providing
electrical connections from the
chips to an exterior of the packag
Inventor: Honda; Tosiyuki et al.
Assignee: Fujitsu Limited et al.
Abstract:

A chip-on chip type semiconductor device is provided in which semiconductor chips provided in a package cannot be displaced during a transfer molding process so as to eliminate a short circuit. At least two lead frames are provided in and extend from the package so that the first semiconductor chip and the second semiconductor chip can be electrically connected to external devices. A die stage is provided between the first semiconductor chip and the second semiconductor chip. A bonding wire is provided for wiring between the first semiconductor chip and the lead frames, and TAB leads connect the second semiconductor chip to the lead frames. The lead frames may extend between the first and second semiconductor devices instead of the die stage. The lead frames may

include one having a portion extending in a direction perpendicular to the longitudinal direction of the lead frames between the first and second semiconductor chips.

20 05614441 Mar 25 1997 29/827 Process of folding a strip
May 4 1995 leadframe to superpose two leadframes in a plural semiconductor die encapsulated package

Inventor: Hosokawa; Ryuji et al.
Assignee: Kabushiki Kaisha Toshiba
Abstract:

A method of manufacturing a semiconductor device wherein, a first lead frame portion has a bed portion for mounting a semiconductor element and a plurality of inner and outer leads. A second lead frame portion has a bed portion for mounting a semiconductor element and a plurality of inner and outer leads as in the first lead frame portion coupled to the second lead frame portion through a coupling portion. The first and second lead frame portions are folded at the coupling portion and superposed such that the two semiconductor elements oppose each other. At this time, the plurality of inner and outer leads of the first and second lead frames are alternately and adjacently arranged. Each electrode of the semiconductor elements is connected to a corresponding inner lead. The superposed first and second lead frames are sealed with a mold resin while leaving end portions of the plurality of outer leads of the first and second lead frames.

21 05587606 Dec 24 1996 257/670 Lead frame having deflectable and
Feb 16 1995 thereby precisely removed tie bars

Status: certificate of correction has been issued
Inventor: Sekiba; Takashi
Assignee: Fujitsu Miyagi Electronics Ltd.
Abstract:

A lead frame includes a die pad on which a semiconductor chip is mounted, a plurality of leads each having an end which faces the die pad, and tie bars connecting the leads, wherein each of the tie bars is formed so as to project from a surface of each of the leads by an amount sufficient to break a boundary between a tie bar and a lead when the tie bar is pushed back so that the tie bar and lead is separated. The method for producing a semiconductor device using the above lead frame includes steps of clamping by molding dies the lead frame having the semiconductor chip mounted on the die pad so that the tie bar is pushed back and cut off and encapsulating the semiconductor chip by resin so that a package made of the resin is formed, and releasing the lead frame from clamping by the molding dies and removing the tie bar pushed back by the clamping from the

lead frame.

22 05535509 Jul 16 1996 29/827 Method of making a lead on chip
Oct 19 1994 (LOC) semiconductor device
Inventor: Tomita; Yoshihiro et al.
Assignee: Mitsubishi Denki Kabushiki Kaisha
Abstract:

A semiconductor device including a lead on chip structure employs two frames. One of the frames includes a die pad and an outer frame portion and the other frame includes a plurality of leads and an outer lead portion. After a semiconductor chip is die bonded to the die pad, the two frames are connected to each other with the leads extending across the semiconductor chip. Slits within the second frame provide access to parts of the outer frame of the first frame and the first frame is severed at those slits. The severed portions of the first frame are removed after which the leads of the second frame are connected by wire bonding to the semiconductor chip. Finally, the semiconductor chip, the remaining part of the first frame, and the second frame are encapsulated in a resin with leads extending from the resin. The remaining parts of the outer frame of the second frame are removed by cutting and the exposed leads outside the resin are formed into a desired shape.

23 054223314 Jun 6 1995 29/827 Lead frame and production method
Dec 13 1993 for producing semiconductor device
using the lead frame
Inventor: Sekiba; Takashi
Assignee: Fujitsu Miyagi Electronics Ltd.
Abstract:

A lead frame includes a die pad on which a semiconductor chip is mounted, a plurality of leads each having an end which faces the die pad, and tie bars connecting the leads, wherein each of the tie bars is formed so as to project from a surface of each of the leads by an amount sufficient to break a boundary between a tie bar and a Lead when the tie bar is pushed back so that the tie bar and lead is separated. The method for producing a semiconductor device using the above lead frame includes steps of clamping by molding dies the lead frame having the semiconductor chip mounted on the die pad so that the tie bar is pushed back and cut off and encapsulating the semiconductor chip by resin so that a package made of the resin is formed, and releasing the lead frame from clamping by the molding dies and removing the tie bar pushed back by the clamping from the lead frame.

24 05633205 May 27 1997 29/827 Lead frame and process of
Aug 11 1995 producing such a frame
Inventor: Tsuchiya; Kenichiro et al.

Assignee: Shinko Electric Industries Co., Ltd.
Abstract:

A lead frame includes a plurality of inner leads, each of the inner leads having at least one surface defining a bonding area and two opposed side edges. The tip ends of the plurality of inner leads are connected by a connecting part so that the inner leads are arranged side by side with respect to each other. The connecting part is integrally and simultaneously formed with the inner leads by an etching process. Each of the inner leads has recesses on the two side edges at a position, between the bonding area and the connecting part, on a cutting line along which the plurality of inner leads are to be cut and separated into individual inner leads.

25 05424577 Jun 13 1995 257/670 Lead frame for semiconductor device
Mar 30 1994
Inventor: Suzuki; Yasuhito et al.
Assignee: Mitsubishi Denki Kabushiki Kaisha
Abstract:

A lead frame for semiconductor devices which does not require tie bar cutting in the manufacture of semiconductor devices includes a base lead frame having no tie bars and a dummy lead frame having dummy leads filling gaps between outer lead portions of the leads when the dummy lead frame is mounted on the base lead frame. Instead of tie bars, the dummy leads reinforce the leads and also stop molten sealing resin from flowing into the gaps between the outer lead portions during resin molding.

26 05543658 Aug 6 1996 257/676 Method of manufacturing resin-sealed semiconductor device, lead frame used in this method for mounting plurality of semiconductor elements, and resin-sealed semiconductor device
Mar 16 1994
Inventor: Hosokawa; Ryuji et al.
Assignee: Kabushiki Kaisha Toshiba
Abstract:

According to a method of manufacturing a semiconductor device of this invention, a first lead frame portion has a bed portion for mounting a semiconductor element and a plurality of inner and outer leads. A second lead frame portion has a bed portion for mounting a semiconductor element and a plurality of inner and outer leads as in the first lead frame portion coupled to the second lead frame portion through a coupling portion. The first and second lead frame portions are folded at the coupling portion and superposed each other such that the two semiconductor elements oppose each other. At this time, the plurality of inner and outer leads of the first and second lead frames are alternately and adjacently

arranged. Each electrode of the semiconductor elements is connected to a corresponding inner lead. The superposed first and second lead frames are sealed with a mold resin while leaving end portions of the plurality of outer leads of the first and second lead frames.

27 05338705 Aug 16 1994 29/827 Pressure differential downset
Sep 10 1992
Inventor: Harris; Guy et al.
Assignee: Texas Instruments Incorporated
Abstract:
The edges of a semiconductor die are moved away from the lead frame leads attached to the die by using a pressure differential across the semiconductor die.

28 05481899 Jan 9 1996 72/453.11 Pressure differential downset
Jun 27 1994 apparatus
Inventor: Harris; Guy et al.
Assignee: Texas Instruments Incorporated
Abstract:
The edges of a semiconductor die are moved away from the lead frame leads attached to the die by using a pressure differential across the semiconductor die.

29 05293066 Mar 8 1994 257/668 Semiconductor device mounting
Mar 6 1992 structure including lead frame and lead plate
Status: certificate of correction has been issued
Inventor: Tsumura; Kiyoaki
Assignee: Mitsubishi Denki Kabushiki Kaisha
Abstract:
Leads near a die pad of a lead frame for a semiconductor device include terminal leads in a pattern on an insulating resin layer. The inner ends of the terminal leads are connected with gold wires to electrode pads of a semiconductor chip, and the outer ends of the terminal leads are also connected with gold wires to inner lead portions of the leads. Wide ground pads are provided which extend from the inner lead portions to the die pad. Ground electrodes on the semiconductor chip are connected with wires to the ground pads to which the insulating resin layer is bonded.

30 04504435 Mar 12 1985 264/272.17 Method for semiconductor device
Oct 4 1982 packaging
Inventor: Orcutt; John W.
Assignee: Texas Instruments Incorporated
Abstract:

A method and apparatus for encapsulating a lead frame in a flat metal strip and a semiconductor device attached thereto having a mold receiving the semiconductor device and lead frame into a cavity. The strip has a thoroughfare over a solid surface to adjacent said lead frame. A depression in the mold over a portion of the thoroughfare contains a pellet of plastic. A runner extends from the depression over the thoroughfare to transfer liquid plastic from the depression into the cavity.

31 05729049 Mar 17 1998 257/666 Tape under frame for conventional-
Mar 19 1996 type IC package assembly
Inventor: Corisis; David J. et al.
Assignee: Micron Technology, Inc.
Abstract:

A semiconductor integrated circuit device, and method of manufacturing the same, having a conventional-type lead frame with the die paddle removed. In particular, the die paddle is replaced with a section of tape that is supported by the ends of the lead fingers. The semiconductor die is attached to the tape so that it may be wire bonded to the lead fingers. The tape contains at least one slot to allow for expansion and/or contraction of the tape due to various temperatures experienced during the manufacturing process so that the tape does not wrinkle or warp to alter the position of the die.

32 05291059 Mar 1 1994 257/666 Resin-molded semiconductor device
Sep 11 1992 and lead frame employed for
fabricating the same
Inventor: Ishitsuka; Masahiro et al.
Assignee: Mitsubishi Denki Kabushiki Kaisha
Abstract:

A semiconductor device has a lead, an inner lead of which is upwardly bent while an outer lead is downwardly bent. A junction part of the outer lead is guided from a resin block on a level which is lower than that of an upper major surface of the semiconductor chip. In fabrication of this semiconductor device, a guide frame of a lead frame, a suspending lead and a die pad held by the same are flush with each other.

33 04919857 Apr 24 1990 264/496 Method of molding a pin holder on
Aug 25 1988 a lead frame
Inventor: Hojyo; Tetsuya
Abstract:

A method of molding a pin holding structure on a lead frame having a plurality of inner lead pins associated with an island, wherein fluid resinous material is dispensed across successive ones of the inner lead pins and is then hardened while under pressure between flat presser

plates. The resin is high in heat resistance as well as in purity, electrical non-conductivity, and low in linear expansibility.

34 05087590 Feb 11 1992 29/827 Method of manufacturing
Oct 24 1989 semiconductor devices
Inventor: Fujimoto; Hitoshi et al.
Assignee: Mitsubishi Denki Kabushiki Kaisha
Abstract:

With a method of and an apparatus for manufacturing semiconductor devices using copper-type lead frames with no silver plating, semiconductor devices are continuously manufactured in the following steps: first, a semiconductor pellet having electrodes on its surface is bonded, through a resin material, to a die pad on a copper-alloy lead frame which is not silver-plated. The resin material used for the bonding is then cured by heating it for 120 seconds or less in a non-oxidizing-gas atmosphere having an oxygen density of 1000 ppm or less. Then, the thickness of the oxide film which is formed on the surface of the lead frame while curing the resin material is reduced to 20 or less by keeping the lead frame in a deoxidizing-gas atmosphere having an oxygen density of 500 ppm or less. Afterwards, wire-bonding is effected between the electrodes of the semiconductor pellet and the inner leads of the lead frame in 12 seconds or less in a deoxidizing-gas atmosphere while keeping the oxygen density around the surface of the lead frame at 3000 ppm or less.

35 05724726 Mar 10 1998 29/827 Method of making leadframe for
Mar 13 1996 lead-on-chip (LOC) semiconductor device
Inventor: Tomita; Yoshihiro et al.
Assignee: Mitsubishi Denki Kabushiki Kaisha
Abstract:

A method of making a semiconductor device having a lead-on-chip structure includes bending a die pad extending from an outer frame outwardly from the outer frame. Thereafter, with the die pad in a convenient position, a semiconductor chip is die-bonded to the die pad. Thereafter, the die pad is bent back toward the outer frame so that it is generally parallel to but spaced from the outer frame with leads extending from the outer frame being generally parallel to the semiconductor chip. Electrodes of the semiconductor chip are connected by wire-bonding to the leads extending from the outer frame. After resin molding, the outer frame lying outside the resin package is severed and removed, completing the lead-on-chip semiconductor device.

36 05710456 Jan 20 1998 257/666 Silver spot/palladium plate lead
Jun 7 1995 frame finish

Inventor: Abbott; Donald C. et al.
Assignee: Texas Instruments Incorporated
Abstract:
A lead frame is plated with palladium and then selected portions of the lead frame leads are spot plated with silver to improve solderability.

37 04581096 Apr 8 1986 156/513 Tape applying device
Aug 8 1984
Inventor: Sato; Fumio
Assignee: Sumitomo Metal Mining Company Limited
Abstract:
A tape applying device for punching an annular piece out of an adhesive tape and applying the annular piece of adhesive tape to the inner leads of a lead frame having leads which extend outwardly therefrom in four general directions includes an inner pattern punch disposed along the direction of the travel of the adhesive tape on one surface side thereof and an outer pattern punch disposed along the direction of the travel of the adhesive tape on the same side as the inner punch on the downstream side relative to the inner punch. The outer pattern punch is provided with a press mechanism for applying under pressure the annularly shaped piece of the adhesive tape to the inner leads of the lead frame.

38 04951119 Aug 21 1990 257/666 Lead frame for semiconductor
Feb 8 1989 devices
Inventor: Yonemochi; Kazuto et al.
Assignee: Shinko Electric Industries, Co., Ltd.
Abstract:
A lead frame for semiconductor devices comprises a plurality of lead sets, each made of a metal strip of a plurality of leads arranged side by side with a small clearance therebetween and a connecting member for integrally connecting the leads. A plurality of such lead sets are arranged in desired positions with respect to each other to form a lead frame assembly.

39 05230144 Jul 27 1993 29/827 Method of producing lead frame
Mar 16 1992
Inventor: Ootsuki; Tetsuya
Assignee: Seiko Epson Corporation
Abstract:
A lead frame having inner leads which secures predetermined mechanical strength and which has no possibility of generation of twisting or the like through working, and a method of producing such a lead frame.

40 05358598 Oct 25 1994 216/14 Folded bus bar leadframe and
Jan 26 1994 method of making

Inventor: Chiu; Anthony M.
Assignee: Texas Instruments Incorporated
Abstract:
A leadframe has a bus bar extending between two lead fingers on the leadframe. The bus bar and lead fingers are etched to reduce the thickness thereof, and the bus bar is folded under the lead finger, but insulated therefrom by a strip of insulating material. An adhesive is applied to the bus bar to attached it and the leadframe to the surface of a semiconductor chip.

41 05444293 Aug 22 1995 257/666 Structure and method for providing
Sep 22 1993 a lead frame with enhanced solder wetting leads

Inventor: Li; Tung L.
Assignee: QPL Limited
Abstract:
A lead frame for used in a surface mount package is provided leads which are each notched at the tip of the lead to reduce the exposed area of based metal and to increase the area on which solder wetting can take place when bonded to conductive traces of a printed circuit board. In one embodiment, the thickness of the tip of the lead is reduced to further the area over which soldering wetting takes place. In that embodiment, the exposed base metal area is reduced by 85 percent.

42 05531860 Jul 2 1996 29/827 Structure and method for providing
May 4 1995 a lead frame with enhanced solder wetting leads

Inventor: Li; Tung L.
Assignee: QPL Limited
Abstract:
A lead frame for used in a surface mount package is provided leads which are each notched at the tip of the lead to reduce the exposed area of based metal and to increase the area on which solder wetting can take place when bonded to conductive traces of a printed circuit board. In one embodiment, the thickness of the tip of the lead is reduced to further the area over which soldering wetting takes place. In that embodiment, the exposed base metal area is reduced by 85 per cent.

43 04870474 Sep 26 1989 257/669 Lead frame
Dec 2 1987

Inventor: Karashima; Akira
Assignee: Texas Instruments Incorporated
Abstract:
A lead frame composed of an outer frame and inner lead frame portions formed as an integral frame wherein each lead frame portion directly joins

the outer frame at some of the four corners of the lead frame portion with circuitous bridges interposed for fixation of the lead frame portion to the outer frame at each of the other corners.

44 05286999 Feb 15 1994 257/666 Folded bus bar leadframe
Sep 8 1992
Inventor: Chiu; Anthony M.
Assignee: Texas Instruments Incorporated
Abstract:
A leadframe has a bus bar extending between two lead fingers on the leadframe. The bus bar and lead fingers are etched to reduce the thickness thereof, and the bus bar is folded under the lead finger, but insulated therefrom by a strip of insulating material. An adhesive is applied to the bus bar to attach it and the leadframe to the surface of a semiconductor chip.

45 05696029 Dec 9 1997 1/1 Process for manufacturing a lead
May 15 1996 frame
Inventor: Alvarez; Robert et al.
Assignee: Texas Instruments Incorporated
Abstract:
A lead frame design and manufacturing process comprising a lead frame (18) having its internal lead fingers (20) punched out to dimensions optimized to accommodate the body size of a selected die. A die pad (30), also optimized to accommodate the body size of the selected die, is attached to the lead frame with mechanical or chemical bonding. Punches are used to punch out the internal lead pins according to selected dimensions.

46 05227662 Jul 13 1993 257/676 Composite lead frame and
Oct 9 1992 semiconductor device using the
same
Status: certificate of correction has been issued
Inventor: Ohno; Yasuhide et al.
Assignee: Nippon Steel Corporation
Abstract:
A composite lead frame comprising a lead frame (10), leads (28) supported on a plastic film (22 ') having a device hole (24), and a metal (14, 32) for mounting a semiconductor chip (34) is disclosed. The lead frame (10) has a plurality of inner lead portions (12) each of which is bonded to each of the leads (28), respectively. The metal (14, 32) also supports the leads (28) through the plastic film (22'). The metal (14, 32) may be bonded to the lead frame (10) through an adhesive tape (16), or may be integrated with the lead frame (10). Bonding wires (36) to connect the leads (28) and the semiconductor chip (34) can be easily and securely

bonded to the leads (28) in virtue of the metal (14, 32) supporting the leads (28). Additionally, a semiconductor device incorporating the composite lead frame has efficient heat dissipation and reliability by virtue of the metal pad.

47 04362902 Dec 7 1982 174/52.4 Ceramic chip carrier
Mar 27 1981
Status: expired - failure to pay third maintenance fee
Inventor: Grabbe; Dimitry G.
Assignee: AMP Incorporated
Abstract:
A semiconductor chip carrier having a lead frame wherein the ends of each of the inner lead portions, which are closely adjacent to the semiconductor device to which the leads are to be bonded, are manufactured with the inner leads temporarily connected to a common supporting rim which must be removed after the attachment of the lead frame to the ceramic substrate is completed. This provides accurate and constant spacing between the leads of the lead frame during the bonding of the lead frame to the ceramic substrate. The rim is removed from the lead frame after bonding of the lead frame to the ceramic substrate. This is accomplished by reducing the thickness of the rim and a portion of the leads of the lead frame contacting and closely adjacent to the rim. This provides a space between the rim and the substrate during the bonding of the lead frame to the substrate. In this way, the rim and a small portion of the leads do not bond to the substrate, thereby allowing the rim to be later removed quite easily.

48 04721994 Jan 26 1988 257/671 Lead frame for semiconductor
Jun 12 1986 devices
Status: expired - failure to pay second maintenance fee
Inventor: Mine; Katsutoshi et al.
Assignee: Toray Silicone Co., Ltd.
Abstract:
This invention provides a semiconductor device lead frame comprising a mounting tab for a semiconductor chip located within the lead frame and multiple inner leads extending to the area adjacent to the perimeter of the tab. The configuration of the inner leads with respect to one another and the mounting tab is stabilized by adhering at least a portion of the leads and, optionally, the mounting tab to a dielectric film coated on one side with a cured, heat-activated silicone adhesive.

49 05173338 Dec 22 1992 427/287 Lead frame workholder and
Apr 4 1991 transport apparatus and method
Status: expired - failure to pay first maintenance fee
Inventor: Sharp; James B. et al.

Assignee: AK Technology, Inc.
Abstract:

Lead frame workholder and transport apparatus for holding and transporting a strip of lead frames from one station to another, each lead frame having a pad and a locating pinhole, comprises a track having an input station at one end and an output station at the other end with an application station in between, a vacuum loader for loading a strip of lead frames onto the input station, a first transporter for contacting the lead frame strip in the input station by inserting a pin into the locating pinhole and moving the strip along the track to the application station, and a second transporter for moving the strip to the output station and into an exit carrier. A method of applying an epoxy layer to the pads of a strip of lead frames using the apparatus is disclosed.

50 05708295 Jan 13 1998 257/676 Lead frame and method of manufacturing the same, and resin sealed semiconductor device and method of manufacturing the same
Apr 26 1996

Inventor: Oga; Akira et al.
Assignee: Matsushita Electronics Corporation
Abstract:

In a space surrounded by outer frames formed in the shape of as rectangle is disposed a die pad in the shape of a square for mounting a semiconductor chip having electrodes. Each of the outer frames is connected with a plurality of outer leads respectively continuous with inner leads which are used for electrical connection and extended toward the die pad. Each inner lead is extended to the vicinity of a position where each electrode of the semiconductor chip is to be formed. The corners of the die pad are respectively provided with support members extending to positions away from a dam bar by a predetermined distance. The support members are connected with the inner leads via a square ring-shaped insulating member. Thus, the die pad is supported by the outer frames via the support members. Since there is no need to provide a die pad lead, the space at the corner conventionally occupied by the die pad lead can be utilized for wiring, and the leads can be easily led in.

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